

PV Energy Conversion and System Integration

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PV Energy Conversion & Integration

Goal:

Develop a *Plug'N'Gen* solar power architecture for decentralized, low-cost, mass-produced, PV panel-mounted micro-inverters

Tasks:

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- Low cost and ultra-compact PV inverter packages
- Advanced digital control algorithms
- Novel inverter topology and control concepts
- SmartTie interface with the utility grid
- Partners: Petra Solar
- Lead Team: UCF (Florida PEC)
- Budget: \$1,267k





PV Energy Conversion Systems

Grid-tie PV Systems

- Accounts for ~85% of PV market
- □ Do not necessarily need backup energy storage

□ Prices:

- Solar electricity costs: 21-38 ¢/kWhr
- Installation costs: \$5-\$9 per peak Watt





New PV System Architectures

- The inverter technology drives the PV power system architecture
- Presently, the market is dominated by:
 - String inverter PV systems
 - Multi-string inverter systems
- New PV system architectures can greatly impact overall PV system costs
 - Micro inverters
 - □ AC PV modules (*Plug'N'Gen*)





String Inverter PV Systems







Limitations of String Inverter Systems

Non-flexible architecture

- Fixed size systems
- Single point of failure (inverter)

Single MPPT process

Susceptible to single panel damage / shading

Hazardous

• High-voltage strings \rightarrow Arcing potential

Complex system design

String sizing; module matching: direction, shading, ageing

Costly Installation

- Special installation codes and procedures; certified installers
- DC disconnects and wiring conduit





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AC PV Module



FESCE Florida Energy Systems Consortium No DC wiring, disconnects, and bypass diodes True plug-n-play system



AC PV Module Features

Plug'N'Gen Installation & Operation

• Simple installation \rightarrow Installable by any electrician / consumer - DIY

Lower Acquisition & Installation Costs

- No special wiring or installation procedures
- No DC wiring, DC disconnects, DC fuses, bypass diodes, ...

Single Panel MPPT process

Optimal energy harness from each panel

Redundant Operation

No Single Point Failure

Very Safe

- No high voltage DC \rightarrow No accessible DC wiring
- Automatically disconnects once the main power switch is turned off





Increased Energy Harvest







Increased Energy Harvest





output by 10% to 50%



Project Tasks

I. Advanced Digital Control

Optimal pulse skipping control to improve light load efficiency

II. System Integration

- Integration & packaging of DC/DC & Magnetics
- □ Thermal modeling & design





Advanced Digital Control

New advanced digital control techniques were developed to improve solar inverters' efficiency

Background

The California Energy Commission (CEC) efficiency is a weighted efficiency given by:

$$\begin{split} \eta_{CEC} &= 0.04 \cdot \eta_{10\%} + 0.05 \cdot \eta_{20\%} + 0.12 \cdot \eta_{30\%} \\ &+ 0.21 \cdot \eta_{50\%} + 0.53 \cdot \eta_{75\%} + 0.05 \cdot \eta_{100\%} \end{split}$$

Maximizing the CEC efficiency necessitates a flat efficiency curve





Efficiency Optimization







Efficiency Optimization

- For solar inverters, at low insolation levels (low input power) the inverter efficiency drops dramatically
 - Reduces CEC efficiency
 - □ Need to improve the efficiency at low input power





Pulse Skipping Strategy

- **Goal:** Improve light load & CEC efficiency
- Approach: Store energy from PV in DC bus capacitor then deliver it to the grid at the maximum efficiency point





Optimal Pulse Skipping Control

Pulse skipping control strategy development

- Mathematical loss model
- Model verification
- Optimization for pulse skipping
- Simulation results
- Experimental verification





Loss Model Derivation





Loss Model Derivation

Component	Items	Mathematical expression
Mosfet	Conduction Loss	$P_{conduction_loss} = R_{on} \times I_{RMS}^2$
	Switching loss	$\begin{split} P_{switch_{loss}} &= \frac{1}{2} C_{oss} U_{dc}^2 f_s + (C_{oss} + C_d) U_{dc}^2 f_s + \frac{1}{4} U_{dc} I_L t_{on} f_s \ \ when \ \ I_L > I_s \\ P_{switch_{loss}} &= \frac{1}{2} C_{oss} U_{dc}^2 f_s + (C_{oss} + C_d) U_{dc}^2 f_s + \frac{1}{2} ((C_{oss} + 2C_d) (U_{dc} - \frac{I_L t_{deadisms}}{(C_{oss} + 2C_d)})^2) f_s \\ &+ \frac{1}{4} U_{dc} I_L t_{on} f_s \ \ \ when \ \ \ I_L < I_s \end{split}$
	Driving loss	$E_{charge} = \frac{1}{2} \mathcal{Q}_g V_{gs} \qquad P_{charge} = E_{charge} f$
Driver IC	Quiscent loss	$P_{driver_loss} = I_{quiscent} U_{auxillary}$
Inductor losses	Core loss	$P_{core_loss} = P_V \times core volume(mm^3)$
	Rdc loss	$P_{Rdc} = R_{dc} I_{RMS}^2$
	Rac loss	$P_{Rdc} = R_{dc} I_{ac_RMS}^2$
Sic diode	Forward conduction loss	$P_{Sic_D} = \frac{1}{T_S} \int_{t_0}^{1} I_0 U_{Sic_d} dt = DI_o U_{Sic_d}$
	Reverse recovery loss	0
Diode	Forward conduction loss	$P_{Schoktty_D} = \frac{1}{T_S} \int_{t_1}^{t_2} I_0 U_{Schoktty_d} dt = (1-D) I_o U_{Schoktty_d}$
EMI filter	Copper losses	$P_{EMI} = R_{EMI} I_{RMS}^2$





Model Verification

 Mathematical model was verified against an actual micro inverter







Pulse Skipping Parameters

Power level to start pulse skipping

Power level of pulse

Optimal DC voltage ripple







Optimization Results



- Optimum Power Level to Start Pulse Skipping: 70W
- Optimum Pulse Power: 150W

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Optimum DC Voltage Ripple: Insignificant



Efficiency Improvement



At a pulse power level of pulse 150W





Efficiency Improvement

- CEC efficiency can be improved by 0.5%-1% using newly develop digital control schemes
 - □ No cost impact on AC module
 - □ Maximized energy output at low insolation levels

